LOW POWER ADIABATIC LOGIC CIRCUITS ANALYSIS

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ABSTRACT

In this paper we are going to compare the adiabatic logic designs & designing a new full adder using ECRL & PFAL logics after that the simulations were done using Micro wind & DSCH. Thus the efficiency of the circuits is shown & compared using different Nano meter technologies. Adiabatic Logic Circuits are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the critical path that determines the overall performance of the system. In this paper conventional complementary metal oxide semiconductor (CMOS) and adiabatic logic circuits are analyzed in terms of power and transistor count using 0.18µm UMC technology.

Keywords: Adiabatic, ECRL Logic, GFCAL Logic, Positive Feedback Adiabatic Logic.

I INTRODUCTION

The main objective of this research is to provide new low power solutions for Very Large Scale Integration (VLSI) designers. Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies. Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

Furthermore, the number of gates per chip area is constantly increasing, while the gate switching energy does not decrease at the same rate, so the power dissipation rises and heat removal becomes more difficult and expensive. Then, to limit the power dissipation, alternative solutions at each level of abstraction are proposed.

The dynamic power requirement of CMOS circuits is rapidly becoming a major concern in the design of personal information systems and large computers. In this thesis work, a new CMOS logic family called *ADIABATIC LOGIC*, based on the adiabatic switching principle is presented. The term adiabatic comes from thermodynamics, used to describe a process in which there is no exchange of heat with the environment. The adiabatic logic structure dramatically reduces the power dissipation. The adiabatic switching technique can achieve very low power dissipation, but at the expense of circuit complexity. Adiabatic logic offers a way to reuse the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and wasting this energy.

This research work demonstrates the low power dissipation of Adiabatic Logic by presenting the results of designing various design/ cell units employing Adiabatic Logic circuit techniques. A family of full-custom conventional CMOS Logic and an Adiabatic Logic units for example, an inverter, a two-input NAND gate, a two-input NOR gate, a two-input XOR gate, a two-to-one multiplexer and a one-bit Full Adder were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μmtechnology, laid out in Micro wind IC Station. All the circuit simulations has been done using various schematics of the structure and post-layout simulations are also being done after they all have been laid-out by considering all the basic design rules and by running the LVS program. Finally, the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done to show the amount of power dissipated by the two logic families.

II MOTIVATION

In the past few decades ago, the electronics industry has been experiencing an unprecedented spurt in growth, thanks to the use of integrated circuits in computing, telecommunications and consumer electronics. We have come a long way from the single transistor era in 1958 to the present day ULSI (Ultra Large Scale Integration) systems with more than 50 million transistors in a single chip.

The ever-growing number of transistors integrated on a chip and the increasing transistor switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint. For example, high-end microprocessors in 2010 are predicted to employ billions of transistors at clock rates over 30GHz to achieve TIPS (Tera Instructions per seconds) performance [1]. With this rate, high-end microprocessor's power dissipation is projected to reach thousands of Watts. This thesis investigates one of the major sources of the power/energy dissipation and proposes and evaluates the techniques to reduce the dissipation. The word *ADIABATIC* comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as *ENERGY RECOVERY CMOS* .

It should be noted that the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

Here, the load capacitance is charged by a constant-current source (instead of the constant-voltage source as in the conventional CMOS circuits).

Here, *R* is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage *VC* is zero initially.

III ADIABATIC PRINCIPLE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail.

3.1 Conventional Switching

There are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance . The equivalent circuits of CMOS logic for charging and discharging is shown in Fig.1.

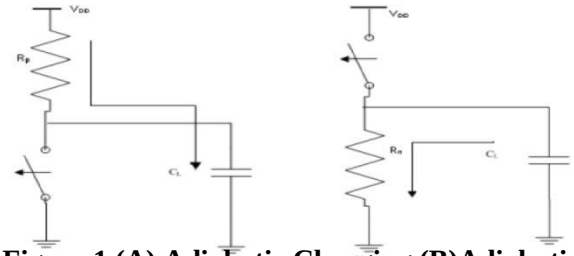

Figure 1 (A) Adiabatic Charging (B)Adiabatic Discharging

The expression for total power dissipation is given by,

$$P_{tot} = \alpha . C_L . V . V_{DD} . f_{clk} + I_{SC} . V_{DD} + I_{le} . V_{DD} \quad \text{----------(1)}$$

Equation (1), the first term represents the dynamic power, where $\boldsymbol{C_L}$ is the loading capacitance, $\mathbf{f_{clk}}$ is the clock frequency, and α is the switching activity. In most cases, the voltage swing V is the same as the supply voltage $V_{dd;}$ however, in some logic circuits, the voltage swing on some internal nodes may be slightly less. The second term is due to the direct- path short circuit current I_{sc} which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. Finally, leakage current I_{le} which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations.

3.2 Adiabatic Switching

Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time-varying voltage source or constant current source , as shown in Fig. 2. Here, R represents the on-resistance of the pMOS network. Also note that a constant charging current corresponds to a linear voltage ramp.

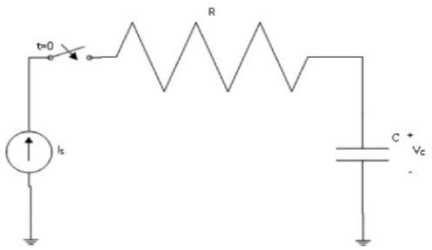

Figure 2 Schematic for adiabatic charging process

Assuming that the capacitance voltage V_C is zero initially, the variation of the voltage as a function of time can be found as

$$V_C(t) = I_S .t / C \quad \text{----------(2)}$$

Hence the charging current can be expressed as a function of V_C and time t

$$I_S = C .V_C(t) / t \quad \text{----------(3)}$$

The amount of energy dissipated in the resistor R from t = 0 to *t* = T can be found as

$$E_{diss} = R\int_0^T I_S^2 dt = RI_S^2 T \quad \text{----------(4)}$$

Combining (3) and (4), the dissipated energy during this charge-up transition can also be expressed as

$$E_{diss} = \frac{RC}{T}.CV_C^2(T) \quad \text{----------(5)}$$

From (5) we can say that the dissipated energy is smaller than for the conventional case if the charging time T >>2RC and can be made small by increasing the charging time. A portion of the energy thus stored in the capacitance can also be reclaimed by reversing the current source direction, allowing the charge to be transferred from the capacitance back into the supply.

Adiabatic logic circuits thus require non-standard power supplies with time-varying voltage, also called pulsed power supplies. The additional hardware overhead associated with these specific power supply circuits is one of the design trade-off. Practical supplies can be constructed by using resonant inductor circuits. But the use of inductors should be limited from integrated circuit point because of so many factors like chip integration, accuracy, efficiency etc.

An alternative to using pure voltage ramps is to use stepwise supply voltage waveforms, where the output voltage of the power supply is increased and decreased in small increments during charging and discharging. Since the energy dissipation depends on average voltage drop across resistor by using smaller voltage steps the dissipation can be reduced considerably . The total dissipation using step wise charging is given by (6)

$$E_{tdiss} = \frac{1}{n} C V_{DD}^2 / 2$$

----------*(6)*

Where n is number of steps used to charge up capacitance to V_{DD}.

IV ADIABATIC LOGIC TYPES

Adiabatic logic circuits classified into two types :

(a) Quasi/Partial Adiabatic Logic Circuits

(b) Full Adiabatic Logic Circuits

(a) Quasi/Partial Adiabatic Logic Circuits :- Quasi-adiabatic circuits have simple architecture and power clock system. The adiabatic loss occurs when current flows through non-ideal switch, which is proportional to the frequency of the power-clock.

(b) Full Adiabatic Logic Circuits :- Full-adiabatic circuits have no non- adiabatic loss, but they are much more complex than quasi-adiabatic circuits. all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuits face a lot of problems with respect to the operating speed and the inputs power clock synchronization. Example:-

4.1 ECERL-Efficient Charge Recovery Logic

Efficient Charge – Recovery Logic (ECRL) proposed by Moon and Jeong , uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling.It consists of two cross-coupled transistors *M1* and *M2* and two NMOS transistors, in the AC power supply *pwr*is used for ECRL gates, so as to recover and reuse the supplied energy. Both *out* and */out* are generated so that the powerclock generator can always drive a constant load capacitance independent of the input signal. A more detailed description of ECRL can be found in. Full output swings is obtained because of the cross-coupled PMOS transistors in both precharge and recover phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the precharge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing.

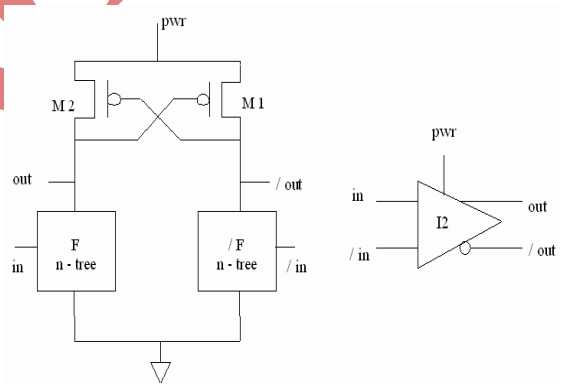

Figure3: The Basic Structure of the Adiabatic ECRL Logic.

So the recovery path to the supply clock to the supply clock is disconnected, thus, resulting in incomplete recovery. *Vtp*is the threshold voltage of PMOS transistor. The amount of loss is given as

$$EECRL = C|Vtp|2 / 2 \text{ ----------} (7)$$

Thus, from Equation ,it can be inferred that the non-adiabatic energy loss is dependent on the load capacitance and independent of the frequency of operation.

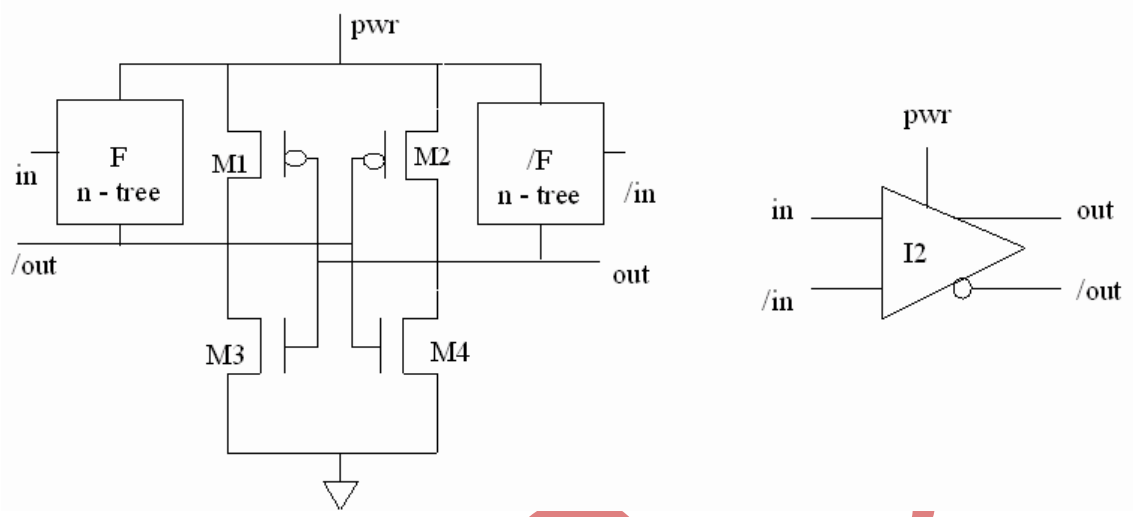

Figure 4: The Basic Structure of the Adiabatic ECRL Logic.

The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETS, rather than by only two PMOSFETs as in ECRL logic, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The energy dissipation by the CMOS Logic family and Adiabatic PFAL Logic family can be seen.

Table1:

Comparison of power, delay and PDP with load capacitance at f_{pc} = 80 MHz and f_{in} = 40 MHz in 10 cycles of charging/discharging.

Inverters	10 fF	30 fF	50 fF	80 fF	100 fF	200 fF
Power dissipation (μW)						
CMOS	1.44	3.93	6.42	10.1	12.7	24.8
Proposed	0.463	1.36	2.35	4	5.18	10.8
Delay (ns)						
CMOS	0.152	0.376	0.601	0.934	1.166	2.275
Proposed	0.187	0.376	0.51	0.691	0.808	1.42
PDP (fJ)						
CMOS	0.219	1.48	3.86	9.43	14.8	56.4
Proposed	0.087	0.511	1.19	2.77	4.19	15.34
Energy saving %						
	60.2	65.4	69.1	70.6	71.6	72.8
Adiabatic gain						
	2.51	2.89	3.24	3.40	3.53	3.67

V POSITIVE FEEDBACK ADIABATIC LOGIC

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 4.3. The core of all the PFAL gates is an adiabatic amplifier, a latch made by the two PMOS *M1-M2* and two NMOS *M3-M4*, that avoids a logic level degradation on the output nodes *out* and */out*. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The functional blocks are in parallel with the PMOSFETs of the adiabatic amplifier and form a transmission gate. The two n-trees realize the logic functions. This logic family also generates both positive and negative outputs.

VI GFCAL INVERTER AND COMPARISON TO OTHER CIRCUITS

GFCAL means glitch free and cascadable adiabatic logic circuits.This circuit consists of one P-channel MOSFET and a diode in parallel with one N-channel MOSFET and a diode, which in turn are connected in series with the loadcapacitance C.

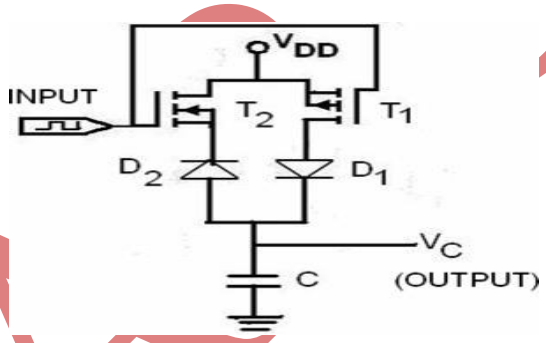

Figure 5:GFCAL Inverter

The supply voltage VDD is a slowly varying triangular voltage.The P-channel MOSFET (T_1) and diode (D_1) provide a charging path, and the N-channel MOSFET (T_2) and diode (D_2) provide a discharging path for the load current.

6.1 Operation of the circuit

When the input is '0' (logic '0'), T_1 is on and T_2 is off. Path T_1, D_1 allows the current flow from the supply and the capacitor becomes charged close to the peak value of V_{DD}, producing logic '1'. The diode D_1 does not allow discharge into the supply when VDD is less than the output voltage. When the input is logic'1', T_2 is on and T_1 is off. The path D_2, T_2 starts conducting. The diode, D_2 prevents charging of the capacitor since it is reverse biased when $V_{DD} > V_C$ and allows only discharging of the capacitor or pumping of energy back into the supply when $V_{DD} < V_C$. Thus, the capacitor voltage is brought down to a low value when the input is high irrespective of the previous output. Hence, the output is the complement of the input.

Features

The output voltage level is almost independent of the time at which the input voltage is applied with respect to the supply voltage as long as it is applied at a time before V_{DD} reaches the peak value.

6.1.1 Energy dissipation in the inverter during charging

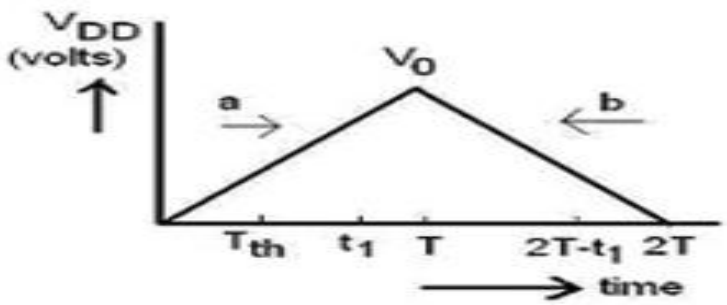

Fig6: Energy dissipation in the inverter

When the P-channel MOSFET is on, and as V_{DD} increases from 0 to Vo, the load capacitor is charged through the diode in the charging path. The voltage reaches a peak value Vo in a time period T and its value $V_{DD}(t)$ at any time 't' is

$$V_{DD}(t) = \frac{V_o}{T} t \qquad \text{when } 0 \le t \le T$$

$$V_{DD}(t) = V_o\left[1 - \frac{(t - T)}{T}\right] \qquad \text{when } T \le t \le 2T$$

The voltage VDD (t) reaches a value VB in a period Tth, when the diode starts conducting. Let Rch be the total resistance in the charging path. The voltage VC across the load capacitor 'C' for t> Tth, is

$$\frac{V_o}{T} t = V_B + R_{ch} C \frac{dV_c}{dt} + V_c$$

Assuming that Tth > CRch, Energy Ech dissipated over the period 0 – T in the diode and the transistor is

$$E_{ch} \approx V_o C(R_{ch} C \frac{V_o}{T} + V_B)(1 - \frac{V_B}{V_o})$$

6.1.2 Energy dissipation in the inverter during discharging

When the N-channel MOSFET is on, the P-channel MOSFET is off, charging of the capacitor is prevented at the load and the capacitor discharges through the diode in the discharge path till t1, that is, till VC is higher than the supply by at least VB, during the period when VDD increases from 0 to Vo. The capacitor then stops discharging at t1 and again continues discharging from 2T–t1 until VC = VB. Let Rdis be the total resistance in the discharging path. Assuming CRdis < t1, the energy Edc dissipated during discharging is the sum of energy dissipated during 0 to t1 and (2T–t1) to 2T which can be shown to be

$$E_{dc} = t_1(2 \frac{V_o^2}{T^2} C^2 R_{dis}) - 2C \frac{V_o}{T} BCR_{dis} + V_B BC + \frac{B^2}{2} C$$

where

$$B = V_{co} - V_B + R_{dis} C \frac{V_o}{T}$$

The total energy E_D, dissipated during one cycle of charging and discharging is given by

$$E_D = E_{ch} + E_{dc} = V_O C(R_{ch} C \frac{V_O}{T} + V_B)(1 - \frac{V_B}{V_O}) + t_1(2\frac{V_\delta^2}{T^2} C^2 R_{dis}) - 2C\frac{V_O}{T} BCR_{dis} + V_B BC + \frac{B^2}{2} C$$

Where t_1 is given by

$$t_1 = R_{dis} C \ln\{\frac{V_{CO} - V_B + (V_O R_{dis}\frac{C}{T})}{V_O R_{dis}\frac{C}{T}}\}$$

Equation (8)

From equation (8)the energy dissipated decreases as T increases. T indicates the rate at which the supply voltage varies and, hence, the energy dissipated decreases with slowly varying the supply voltages. The power dissipation generally changes with parameters like V_O, the value of the capacitance, the equivalent series resistance because of the diode and the MOSFET.

The energy dissipated by different inverters at an input frequency of 25 MHz and a supply frequency of 25 MHz during one cycle of charging and discharging of the load capacitor

Table2: Energy Dissipation in various configurations(25MHz freq)

Type of inverter	Energy dissipation, J
CMOS	9.12×10^{-14}
GFCAL	4.04×10^{-14}
ADL	3.41×10^{-14}
2N-2N2D	6.64×10^{-14}
QSERL	5.11×10^{-14}
2N-2P	5.21×10^{-14}
2N-2N2P	5.26×10^{-14}
CAL	5.19×10^{-14}

The energy dissipated by different inverters at an input frequency of 125 MHz and a supply frequency of 125 MHz during one cycle of charging and discharging of the load capacitor

Table3: Energy Dissipation in various configurations(125MHz freq)

Type of inverter	Energy dissipated, J
CMOS	9.15×10^{-14}
GFCAL	3.84×10^{-14}
ADL	3.64×10^{-14}
2N-2ND	6.51×10^{-14}

VII CONCLUSION

The research primarily was focused on the design of low power CMOS cell structures, which is the main contribution of this work. The design of low power CMOS cell structures uses fully complementary CMOS logic style and an adiabatic PFAL logic style. The basic principle behind implementing various design units in the two logic styles is to compare them with reference to the average power dissipated by all of them.

A family of full-custom conventional CMOS Logic and an Adiabatic Logic units were designed in Mentor Graphics IC Design Architect using standard TSMC 0.35 μmtechnology, layout them in Micro wind & Digital Schematic and the analysis of the average dynamic power dissipation with respect to the frequency and the load capacitance was done. It was found that the adiabatic PFAL logic style is advantageous in applications where power reduction is of prime importance as in high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants.

With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can be used to reduce the power dissipation of the digital systems. With the help of adiabatic logic, the energy savings of up to 76 % to 90 % can

be reached.Circuit simulations show that the adiabatic design units can save energy by a factor of 10 at 50 MHz and about 2 at 250 MHz, as compared to logically equivalent conventional CMOS implementation.

VIII FUTURE WORK

8.1 Adiamems: To perform digital logic in CMOS in a truly adiabatic (asymptotically thermodynamically reversible) fashion requires that the logic transitions be driven by a quasi-trapezoidal (flat-topped) power-clock voltage waveform, which must be generated by a resonant element with very high *Q* (quality factor). Recently, MEMS resonators have attained very high frequencies and *Q* factors and are becoming widely usedin communications system-on-chip (SOC) for RF signal filtering, amplification, etc.

8.2 Application Of Nano-Technology: Carbon Nano-tubes grown using Chemical Vapour Deposition (CVD) can be selected to conform to a spiralling shape. Thus, a good quality factor *Q* can be achieved. The work left to be done for this design would include a method for causing it to keep its form, since Nano-tubes are typically not rigid. Also, putting the tube to use in a circuit would lower the effective *Q* due to the junction discontinuities.

8.3 Spacecraft: The high cost-per-weight of launching computing-related power supplies, solar panels and cooling systems into orbit imposes a demand for adiabatic power reduction in spacecraft in which these components weigh a significant fraction of total spacecraft weight.

REFERENCES

[1] KAUSHIK ROY, SHARAT C. PRASAD, Low-Power CMOS VLSI Circuit
[2] S.Kang and Y.Leblebici (2003), CMOS Digital Integrated Circuits -
[3] Design, John Wiley & Sons, Inc., 2000.
[4] Analysis and Design, McGraw Hill.
[5] Asymptotically Zero Energy Computing Using Split-Level Charge Recovery Logic (http://dspace.mit.edu/handle/1721.1/7058)
[6] http://en.wikipedia.org/w/index.php?title=Adiabatic_circuit&oldid=539401456
[7] www.electronicsforyou.com
[8] www.isrnelectronics.com
[9] www.mosis.org